REMARKS

Claims 1-3 and 5-9 are pending in the application. Claim 9 has been added in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated **July 25, 2002**.

Objection to the Specification

Regarding antecedent basis in the written specification of "the gate insulating film", it is supported by way of examples on page 2, lines 28-31, page 7, lines 22-23, page 10, lines 12-15, among others.

Regarding antecedent basis in the written specification of "first conductivity type body contact region", it is supported by way of examples on page 12, lines 10-12, page 12, lines 21-22, among others.

Furthermore, the applicant has amended the terms "the gate insulating film" in the current claims 1 and 3, and "that first conductivity type body contact region" in the current claims 2 and 3, to -- a gate insulating film --, and -- a first conductivity type body contact region --, respectively, as shown in the amendment submitted herein.

Therefore, reconsideration and withdrawal of this objection are respectfully requested.

Claim Rejections under 35 USC §102

Claim 4 has been rejected under 35 USC §102(b) as being anticipated by Houston (U.S. Patent No. 5,095,348).

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Houston discloses (see figs. 1-9, col, 7, lines 20-42 and claims 1-3) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of an L-shape 242 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern is provided and a body contact region 246 and a drain region 252 isolated through said crosspiece-shaped conductor pattern, said body contact region being made the same potential as a source region 254."

In making this rejection, the Office essentially copied the claim language of the present invention and selectively inserted parenthetical supports to indicate where the same element is disclosed in Houston. However, among many elements, the Office only provided support for four elements. The Applicant cannot find where the unsupported elements are disclosed in Houston.

Therefore, the claimed invention is not anticipated by Houston. For reasons unrelated to the merit of this Office Action, claim 4 is canceled without prejudice to the subject matter thereof.

Claim 4 has been rejected under 35 USC §102(e) as being anticipated by Erstad (U.S. Patent No. 6,307,237).

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Erstad discloses (see figs. 5-8 and col. 9, lines 29-37) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region 302 isolated from a

semiconductor substrate by a substrate isolation insulating film 383, wherein a gate electrode of asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern or L-shaped gate electrode with trunk 117 and crosspiece 118 is provided and a body contact region 332 and a drain region 326 isolated through said crosspiece-shaped conductor pattern, said body contact region being made the same potential as a source region 330."

It is a firm position of the Office that Erstad discloses an active region 302, an insulating film 383, a body contact region 332, a drain region 326 and a source region 330. However, Erstad discloses that these reference numerals all pertain to elements of a U-gate MOSFET. Therefore, the Office allegation that these reference numerals all pertain to a L-gate semiconductor device is unsubstantiated by Erstad.

Erstad has indeed disclosed a L-gate MOSFET as shown in Figure 5. However, the Applicant cannot find each and every claimed element as specified in claim 1 from Erstad.

Therefore, the claimed invention is not anticipated by Houston. For reasons unrelated to the merit of this Office Action, claim 4 is canceled without prejudice to the subject matter thereof.

Claim 5 has been rejected under 35 USC §102(e) as being anticipated by Pennings et al. (U.S. Patent No. 6,154,091).

One feature of claim 5 resides in that a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern, is provided and at least part of the above crosspiece-shaped conductor pattern functions as an effective gate electrode, together with the above trunk-shaped main gate electrode.

However, claim 5 has been further amended to include "the trunk-shaped main gate electrode

is sandwiched between a source region and a drain region, and at least part of the crosspiece-shaped conductor pattern is also sandwiched between the above source region and the above drain region".

Claim 5 is sufficiently supported by Fig. 14(c) and the description on page 25, last line to page 26, line 5 of the present specification.

According to Pennings et al. (U.S. Patent No. 6,154,091), the crosspiece-shape conductor pattern is sandwiched between "DRAIN" and "BODY", as shown in Fig. 4 of Pennings et al.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Pennings et al disclose in figs. 4-7 an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of an L-shape comprised of a trunk-shaped main gate electrode 10 extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern 12 extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode."

As it is clearly shown, the Office Action merely identified 2 of many claimed elements of the claimed invention in the prior art reference. The Applicant has reviewed Figures 4-7 as asserted by the Office and cannot find the remaining claim elements in the prior art.

Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is thereby not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that the claimed invention patentably distinguishes over the

asserted prior art. Claims dependent thereon, by virtue of inherency, also patentably distinguish over the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

As an effort to assist the Office to determine whether indeed each and every element of the claimed invention is disclosed in the prior art, the following claims with parenthetical blanks are submitted herewith.

5. (Twice Amended) An insulated gate type semiconductor device ( ) comprised of a semiconductor layer ( ) serving as an active region ( ) isolated from a semiconductor substrate ( ) by a substrate isolation insulating film ( ), wherein a gate electrode ( ) of a shape of either one of an L-shape ( ) or asymmetric T-shape ( ) comprised of a trunk-shaped main gate electrode ( ) extending in parallel with respect to said semiconductor substrate ( ), and a crosspiece-shaped conductor pattern ( ) extending in parallel with respect to said semiconductor substrate ( ) and also extending toward the width direction of said main gate electrode ( ) is provided and, said trunk-shaped main gate electrode ( ) is sandwiched between a source region ( ) and a drain region ( ), and at least part of said cross-piece-shaped conductor pattern ( ) is also sandwiched between said source region ( ) and said drain region ( ), and thereby at least part of said crosspiece-shaped conductor pattern ( ) functions as an effective gate electrode ( ).

Claim 5 has been rejected under 35 USC §102(b) as being anticipated by Eimori, et al. (U.S. Patent No. 5,637,899).

One feature of claim 5 resides in that a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern, is provided and at least part of the above crosspiece-shaped conductor pattern functions as an effective gate electrode, together with the above trunk-shaped main gate electrode.

However, claim 5 has been further amended to include "the trunk-shaped main gate electrode is sandwiched between a source region and a drain region, and at least part of the crosspiece-shaped conductor pattern is also sandwiched between the above source region and the above drain region".

Claim 5 is sufficiently supported by Fig. 14(c) and the description on page 25, last line to page 26, line 5 of the present specification.

According to Eimori et al. (U.S. Patent No. 5,637,899), the crosspiece-shaped conductor pattern is sandwiched between first conductivity type source/drain regions (3b, 3c) and second conductivity type channel potential fixing regions (4a, 4b), as shown in Fig. 14 of Eimori et al.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Eimori et al. disclose in figs. 14 and 21-29 an insulated gate type semiconductor device comprised of a semiconductor layer 22 serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film 21, wherein a gate electrode 17 of L-shape comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode."

Again, the outstanding Office Action has selectively pointed to a few elements in the prior art allegedly to be the same as those in the claimed invention. However, the claimed invention contains far more features and elements as those few pointed out by the outstanding Office Action. The Applicant simply cannot find many of the claimed elements and claimed features from the prior art.

Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is thereby not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that the claimed invention patentably distinguishes over the asserted prior art. Claims dependent thereon, by virtue of inherency, also patentably distinguish over the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

As an effort to assist the Office to determine whether indeed each and every element of the claimed invention is disclosed in the prior art, the following claims with parenthetical blanks are submitted herewith.

5. (Twice Amended) An insulated gate type semiconductor device ( ) comprised of a semiconductor layer ( ) serving as an active region ( ) isolated from a semiconductor substrate ( ) by a substrate isolation insulating film ( ), wherein a gate electrode ( ) of a shape of either one of an L-shape ( ) or asymmetric T-shape ( ) comprised of a trunk-shaped main gate electrode ( ) extending in parallel with respect to said semiconductor

substrate ( ), and a crosspiece-shaped conductor pattern ( ) extending in parallel with respect to said semiconductor substrate ( ) and also extending toward the width direction of said main gate electrode ( ) is provided and, said trunk-shaped main gate electrode ( ) is sandwiched between a source region ( ) and a drain region ( ), and at least part of said cross-piece-shaped conductor pattern ( ) is also sandwiched between said source region ( ) and said drain region ( ), and thereby at least part of said crosspiece-shaped conductor pattern ( ) functions as an effective gate electrode ( ).

Claim Rejections under 35 USC §103

Claim 5 has been rejected under 35 USC §103(a) as being unpatentable over Bryant et al. (U.S. Patent No. 6,100,564) in view of Houston (U.S. Patent No. 5,498,882).

One feature of claim 5 resides in that a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern, is provided and at least part of the above crosspiece-shaped conductor pattern functions as an effective gate electrode, together with the above trunk-shaped main gate electrode.

However, claim 5 has been further amended to include "the trunk-shaped main gate electrode is sandwiched between a source region and a drain region, and at least part of the crosspiece-shaped conductor pattern is also sandwiched between the above source region and the above drain region".

Claim 5 is sufficiently supported by Fig. 14(c) and the description on page 25, last line to page 26, line 5 of the present specification.

According to Houston (U.S. Patent No. 5,498,882), the crosspiece-shaped conductor pattern is sandwiched between a drain/source region 3 for a first transistor 2 and a drain/source connection 5 comprised of both an n-type region n+ serving as a drain/source of a second transistor 6 and a p-type region P+ connected to a P- region under gate G which serves as both a body node of the first transistor 2 and a base of a bipolar parasitic transistor 4, as shown in Figs. 2 and 3 of Houston and described in col. 2, lines 42 to 61.

According to Bryant et al. (U.S. Patent No. 6,100,564), the cross-piece-shaped conductor pattern 114 is sandwiched between source/drain regions (211, 212) and both a body contact region 113 and a source/drain mask 213, as shown in Fig. 5 of Bryant et al. and described in col. 3, lines 45-51.

In rejecting the claimed invention, the outstanding Office action has specifically stated in relevant part that:

> "Bryant et al. disclose in figs. 4 and 5 an insulated gate type semiconductor device comprised of a semiconductor layer 103 serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film 102, wherein a gate electrode of T-shape comprised of a trunk-shaped main gate electrode 112 extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern 114 extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode.
>
> Houston discloses in fig. 3 an asymmetric gate electrode of T-shape comprised of a trunk-shaped main gate electrode extending in parallel with respect

> to a semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode.
>
> Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use asymmetric gate electrode of T-shape, sine that would reduce gate capacity."

Therefore, it is a firm position of the Office that the T-shaped gate electrode of 112 of Bryant can be substituted by an asymmetric T-shape electrode of Houston, allegedly for the purpose of reducing gate capacity.

It is respectfully submitted that without any teaching or suggestion of such a substitution, the Office position is nothing more than unsubstantiated hindsight conjecture and the *prima facie* case of obviousness is simply not met.

Section 2143 of the MPEP has specifically stated that:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Therefore, it is both a court position and a Patent Office position that to establish a *prima facie* case of obviousness, 1) there **must be** some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the

reference or to combine reference teachings; 2) there **must be** a reasonable expectation of success; and 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success **must both be** found in the prior art, and not based on applicant's disclosure.

Furthermore, claim 5 has been amended to include "the trunk-shaped main gate electrode is sandwiched between a source region and a drain region, and at least part of the cross-piece shaped conductor pattern is also sandwiched between the above source region and the above drain region", as in the present invention, which is not disclosed in any of the asserted references.

Therefore, should the Office either be unable to identified each and every aspect of the above-mentioned claimed features after taking full consideration of the asserted prior art in a way exactly applied in the outstanding Office action, or the Office recognizes that the rejection simply does not arise to a level objectively fulfilling all three criteria of establishing a *prima facie* case of obviousness, it is respectfully submitted that the obviousness rejection is defective and allowance of the claimed invention is requested.

Prior Art Indicated To Be Pertinent To The Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

Conclusion

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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IN THE CLAIMS:

1. (Twice Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, provided with a T-shaped gate electrode comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode and having a length larger than the width of source and drain regions, and having a thickness of [the] a gate insulating film formed directly under the entire region of the crosspiece-shaped conductor pattern greater than the thickness of the gate insulating film directly under the main gate electrode.

2. (Twice Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a thickness of an insulating film provided on a surface of a first conductivity type semiconductor region positioned at an interface between [that] a first conductivity type body contact region and a second conductivity type source and drain regions is made greater than the thickness of a gate insulating film directly under a gate electrode, said gate electrode being provided on the region except for said body contact region.

3. (Twice Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a buried insulating film thicker than the thickness of the gate insulating film directly under a gate electrode is provided on a surface of a first conductivity type semiconductor region positioned at an interface between [that] a first conductivity type body contact region and a second conductivity type source and drain regions, said gate electrode being provided on the region except for said body contact region.

5. (Twice Amended) An insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate by a substrate isolation insulating film, wherein a gate electrode of a shape of either one of an L-shape or asymmetric T-shape comprised of a trunk-shaped main gate electrode extending in parallel with respect to said semiconductor substrate, and a crosspiece-shaped conductor pattern extending in parallel with respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and, said trunk-shaped main gate electrode is sandwiched between a source region and a drain region, and at least part of said cross-piece-shaped conductor pattern is also sandwiched between said source region and said drain region, and thereby at least part of said crosspiece-shaped conductor pattern functions as an effective gate electrode.

respect to said semiconductor substrate and also extending toward the width direction of said main gate electrode is provided and at least part of said crosspiece-shaped conductor pattern functions as an effective gate electrode.